REMARKS

I. Formal Matters.

Claims 1-13 are all the claims pending in the application. Applicant thanks the Examiner for indicating that the drawings filed on February 13, 2004, are acceptable. Applicant also thanks the Examiner for considering the references cited via the Information Disclosure Statements (IDS) filed on filed August 13, 2004 and on September 27, 2004, as evidenced by his return of respective initialled Forms PTO-1449 to the office of the undersigned.

II. Claims.

The Examiner rejects claims 1-13 as being allegedly anticipated by *Dyer et al.* (U.S. Patent Application No. 2005/0069394) under 35 U.S.C. §102(e).

Claims 1 *Dyer* teaches an adjustable load resistor to match load impedance and an adjustable capacitance for slope matching. The Examiner cites to *Dyer* Fig. 3, R3, as disclosing a replica resistor (OA pages 2 and 4; Dyer [0027], [0028]). Still referring to Fig. 3, the Examiner applies and cites to *Dyer* as follows with respect to the last paragraph of claim 1.

> "... a second point of connection (*Dyer* Fig. 3, between R3 and R4)
> between the replica driver (*Dyer* Fig. 3, Replica DAC ***via R4***) and
> the replica resistor (*Dyer* Fig. 3, R3)
> being connected to a receive side (*Dyer* Fig. 3, To Receiver Sampler)." (OA page 3)

Dyer clearly discloses and the Examiner clearly applies a replica drive connected in series with a resistor (R4), the resistor being connected to the connection to the receive side (Figs. 1 and 3; paragraphs [0027] and [0028]; claim 8).

In contrast, claim 1 requires a common node for the replica driver, a second end of the replica resistor, and a connection to the receive side. *Dyer* teaches a resistor (R4) connected in series to the

replica driver, wherein R4 is connected to a second common node for connecting to the receive side. A second resistor (R3) is connected in series to the output node of the current driver for the transmit signal, wherein R3 is connected to the node for connecting to the receive side. *Dyer* teaches a method of output impedance calibration requiring resistors R3 and R4, each connected to a second common node and connected to a current driver, for transmit signal and replica signal, respectively. *Dyer* fails to disclose a replica driver connected to a second common node, wherein the second common node is for connecting to the receive side. At least for this deficiency, the rejection of claim 1 as being anticipated by *Dyer* under under 35 U.S.C. §102(e), should be withdrawn.

Claim 12. The Examiner similarly rejects claims 12 and 1, applying elements of *Dyer*'s Fig. 3 (OA page 4). Claim 12 requires subject matter analogous to that discussed above in the traversal of the rejection of claim 1, wherein claim 12 requires a replica impedance in place of the replica resistor required by claim 1. An analogous argument asserted in traversal of the rejection of claim 1 is hereby asserted in traversal of claim 12. At least for this deficiency, the rejection of claim 12 as being anticipated by *Dyer* under under 35 U.S.C. §102(e), should be withdrawn.

Claims 2-11 and 13 are asserted as being allowable at least by virtue of their dependence upon an allowable claim.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Amelia F. Morani, Ph.D.
Registration No. 52,049

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: March 23, 2006